Energy Efficient Computing Systems (EECS)

An inter-disciplinary research project at the IME-faculty

PP4EE
3. October 2013
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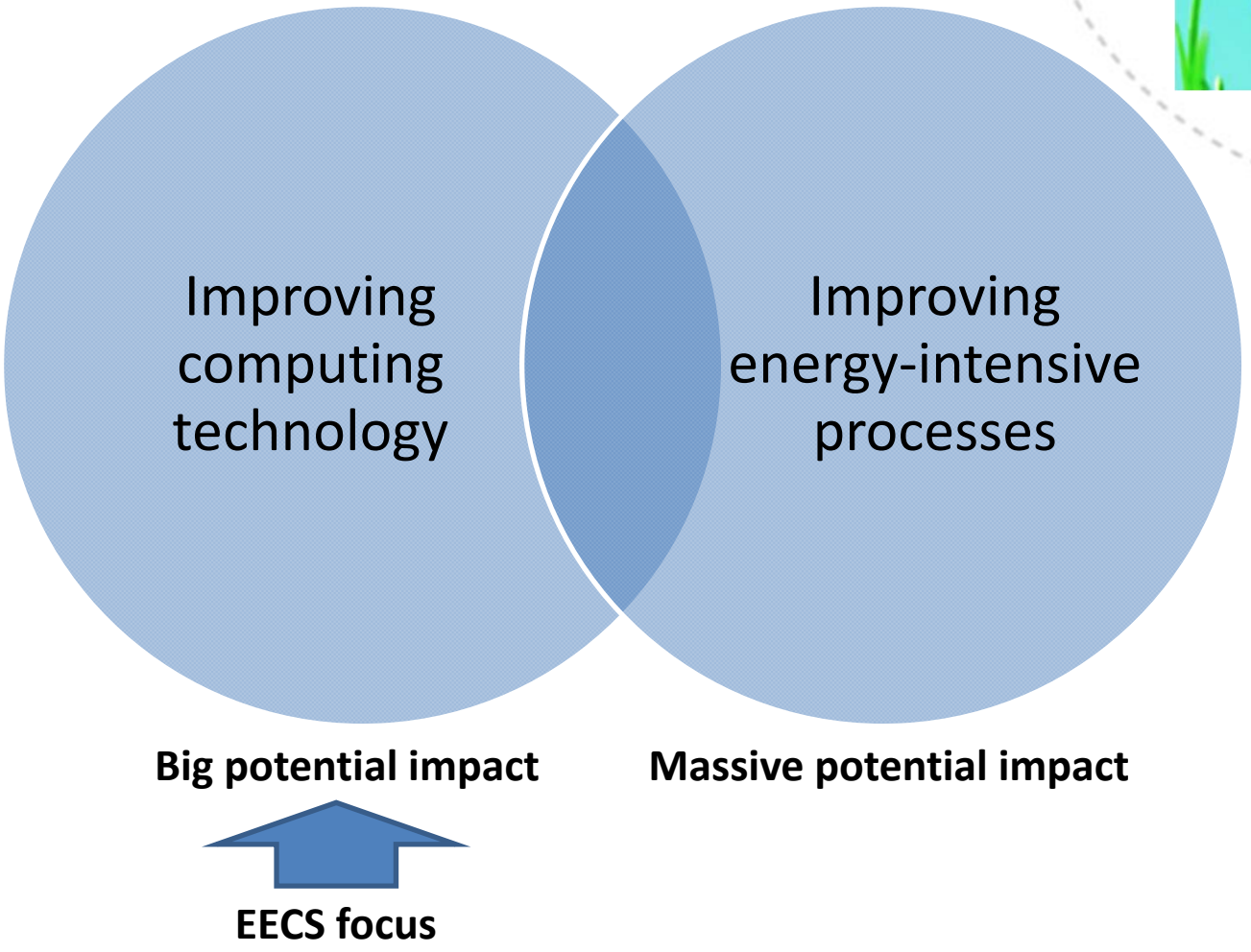
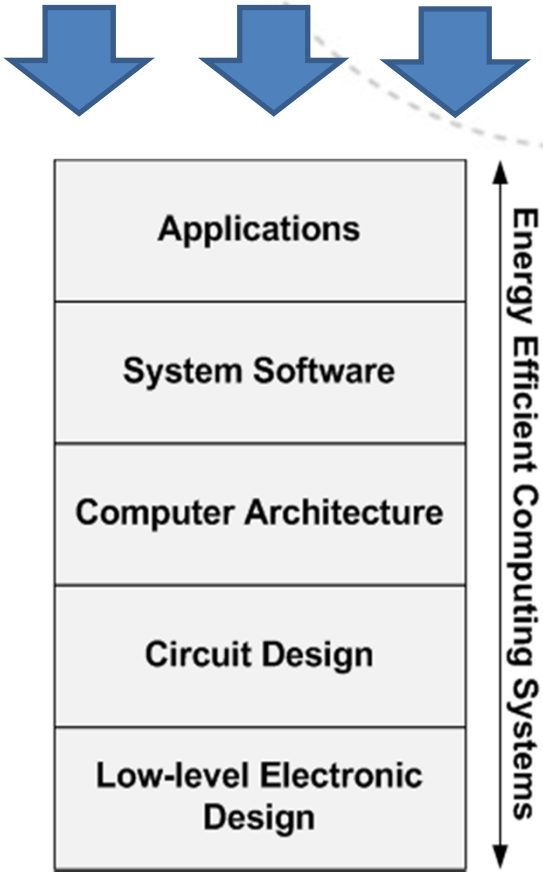
Coordinator, EECS

Green ICT


Improving computing technology
Improving energy-intensive processes
Big potential impact
Massive potential impact
EECS focus

EECS Structure

- Two-level motivation
  - Environmental
  - Technological
- Vertical approach
  - Leverage strong groups working horizontally
- Application agnostic
  - Matches focus of high-volume international industry
  - Choose demonstrator applications that clearly demonstrates proposed innovations



EECS Environmental Motivation

Global Energy Consumption

Other

Computing Systems

Research project goal:
10% reduction

80 TWh

Global Consumer ICT (800 TWh)

Use energy reduction to turn off coal power plants

Norway Total Energy (220 TWh)

Save 80 M metric tones CO_2

Norway annual CO_2: 87M metric tones

Sources: International Energy Agency and SSB

EECS Technical Motivation

Energy efficiency is becoming the primary design goal across all market segments

Extremely energy sensitive systems

- Lifetime of system is equal to battery life
- Lower energy consumption can open new markets

Mobile systems

- Energy: Users want long battery life
- Limited size of cooling system results in strict power constraints

Desktop computers

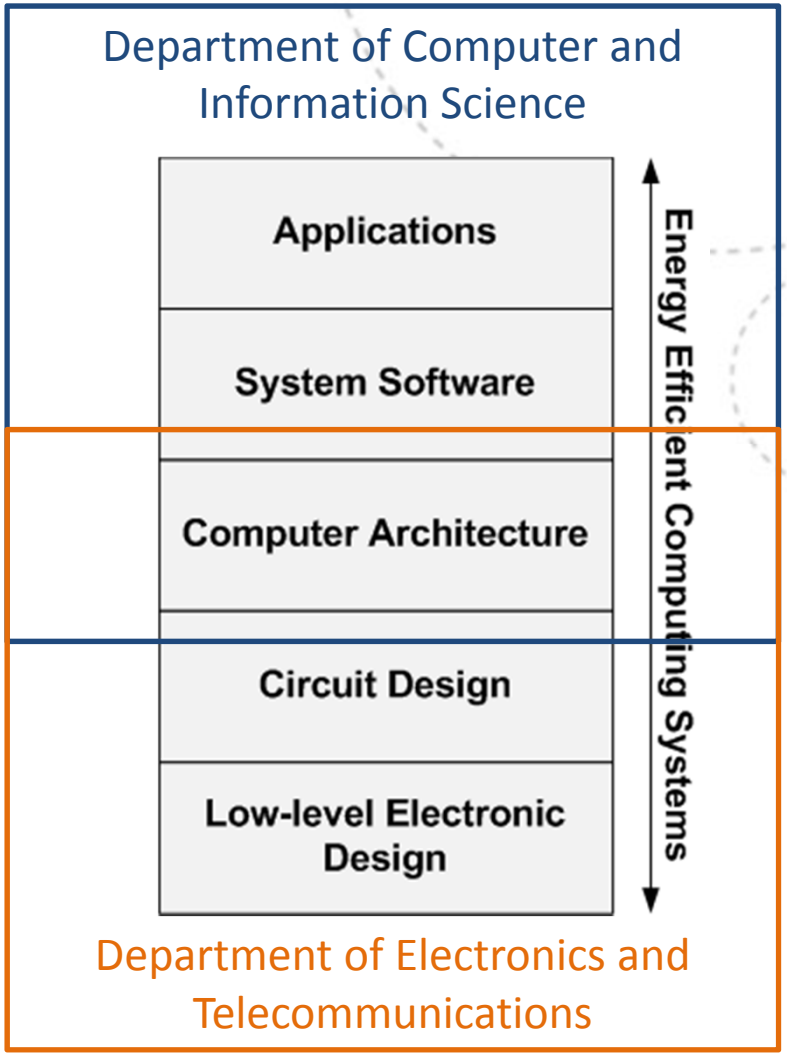
- Fixed power budget due to cooling challenges
- Cannot improve performance without improving energy efficiency

Data centers and HPC

- Energy bill dominates operating cost
- Power consumption is a significant engineering challenge

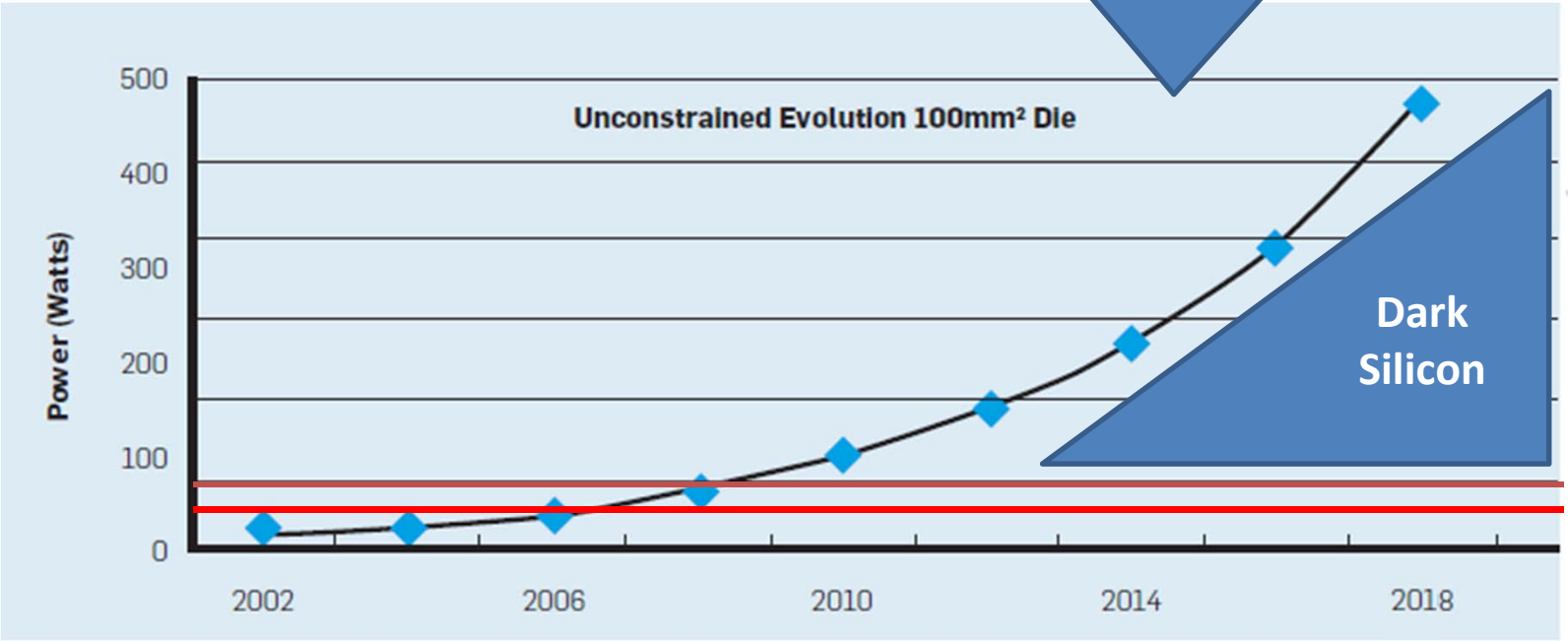
EECS Organization

- Ensuring collaboration:
  - Post Doc. assigned to EECS
  - EECS PhD students will have co-supervisors from other departments
  - Regular EECS research meetings
- Possible future instruments
  - External board/advisory board with industry partners
  - Scientific advisory board
- People
  - 6.2 affiliated permanent staff
  - 10 affiliated PhD students
  - 5 affiliated researchers/lecturers



Business as usual?

Business-as-usual scenario:
Add more cores and increase clock frequency



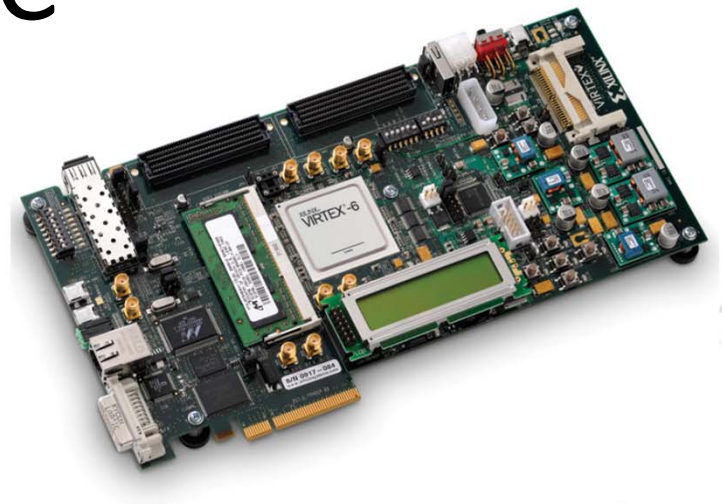
Practical server limit (about 100W)

Practical desktop limit (about 65W)

Paradigm shift from area- to energy-constrained computing

Result: Heterogeneous computing platforms

Vertical Project: SHMAC

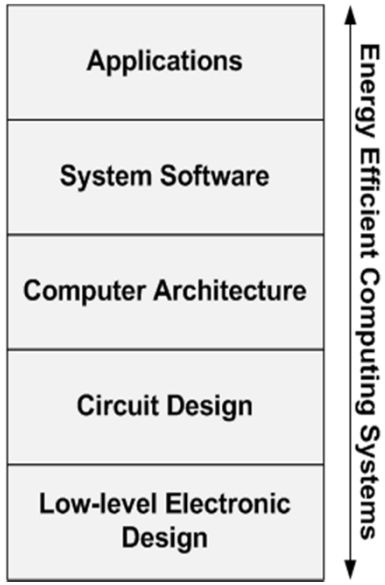


Dark silicon effect makes heterogeneous processors likely

Software for heterogeneous processors is an open research problem

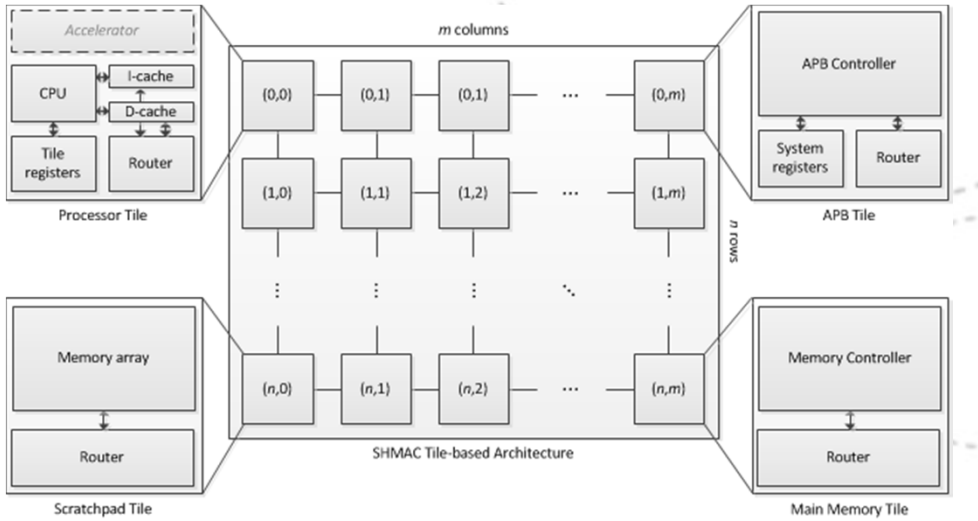
- Heterogeneity of off-the-shelf components is limited
- Simulators have unlimited heterogeneity but are slow

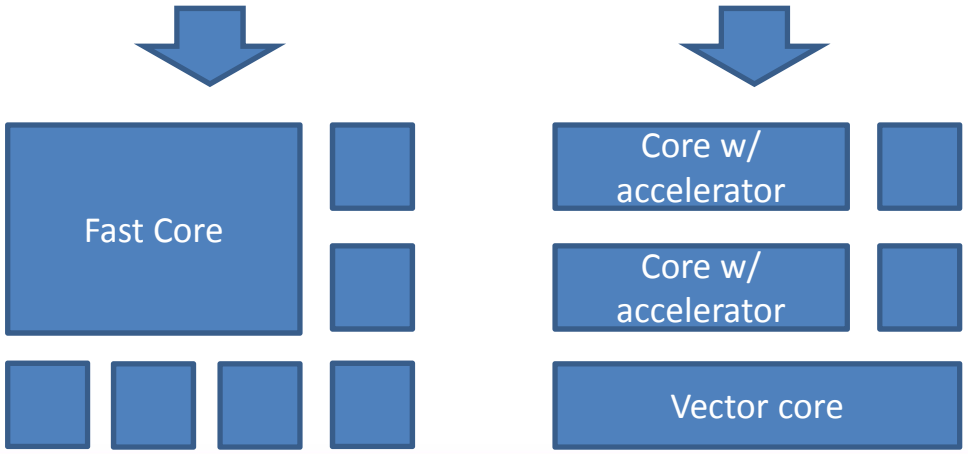
Solution: SHMAC = Single-ISA Heterogeneous MAny-core Computer



SHMAC Architecture

- Tiled multi-core design paradigm describing a class of processor architectures
- Common instruction set and architecture model gives software portability across SHMAC instances
- SHMAC instances can contain various tile types:
  - Processors with different energy/performance characteristics
  - Optimized processors (vector, OOO, etc.)
  - Accelerators





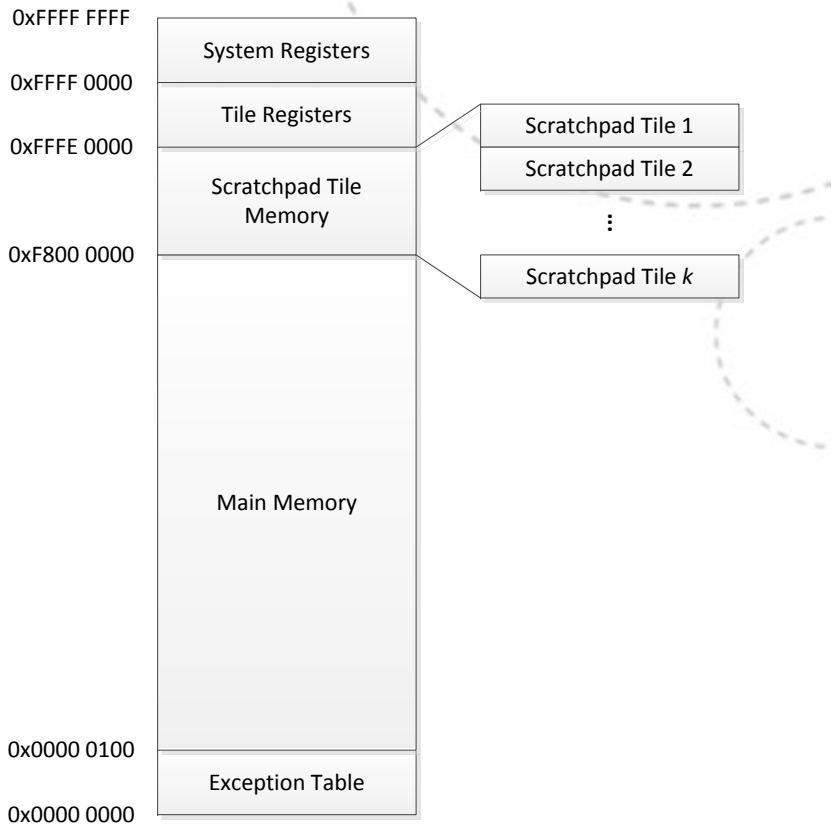
Design Goal: Software Portability

All processor tiles are functionally equivalent

- Performance may be very different
- Different processor classes and accelerators

Uniform architecture

- All processing tiles see the same memory map
- Tile registers are per-tile, other memory locations are global



SHMAC Memory Map

Research question: What are the costs associated with the Single-ISA abstraction?

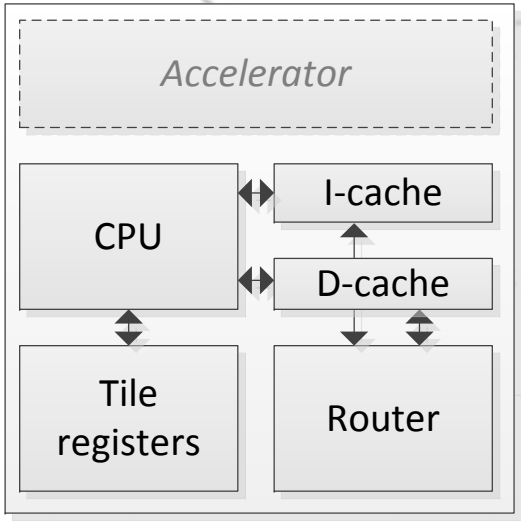
SHMAC Processor Tile

All processor tiles follow a similar high-level architecture

- Processing element implements the ARM ISA
- Tile registers contain data local to the tile
- Non-coherent caches
- Router connects the tile to the Network on Chip (NoC)

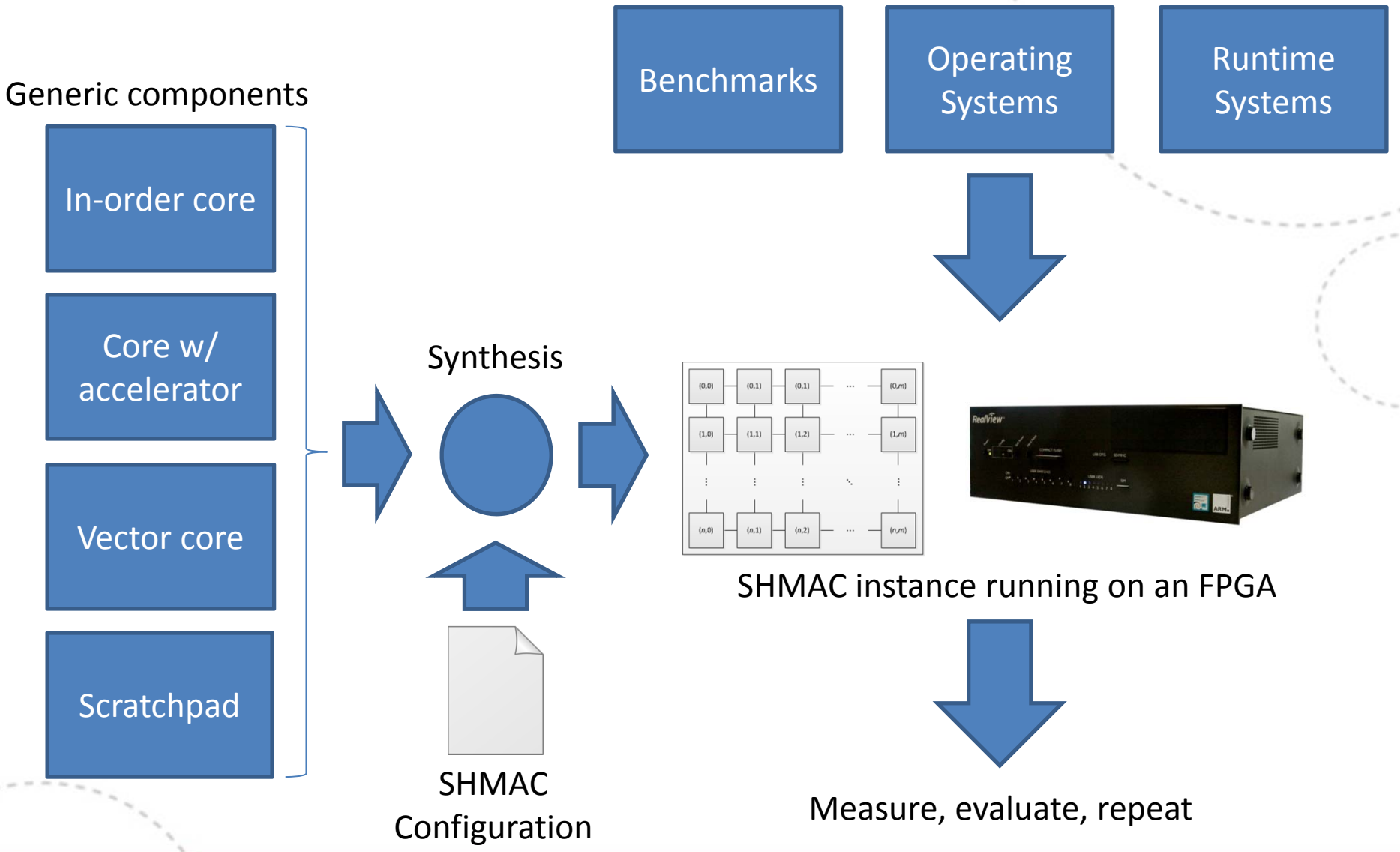
Optional accelerator

- Seamless integration with the rest of the tile
- How to best expose accelerators to the rest of the architecture is current research



Processor Tile

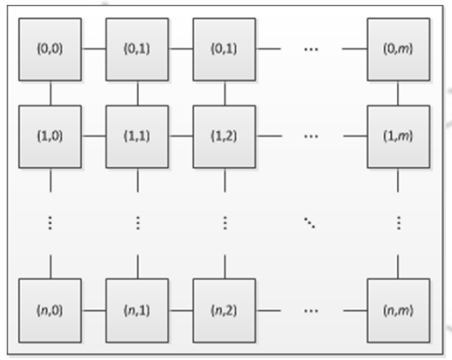
Leveraging Reconfigurability



SHMAC Enables Collaboration

SHMAC combines generic components and powerful abstractions

- Reimplement/extend the part(s) involved in your research project



SHMAC best suited for cross-disciplinary projects where hardware and software innovations are combined

- Different partners can focus on different parts of the system

Possible project examples

- Novel runtime software: Use provided core types to evaluate system across a large range of heterogeneous systems
- Novel microarchitecture: Adapt SHMAC microarchitecture and get software stack for free

EECS is one of seven groups at NTNU that receives special support towards Horizon 2020

Future Directions

Status: Minimal set of tiles to support software development

Future hardware

- Efficient accelerator integration
- Vector core
- Out-of-order core

Future software

- Benchmarks (micro, macro)
- Operating Systems (conventional, multikernel)
- Runtime systems

Significant effort: 1 Post doc., 2 PhD students, 15 master students

Concluding Remarks

EECS Motivation

- Environment: Climate change and efficient use of energy
- Technology: Power consumption limits performance growth across all computing segments

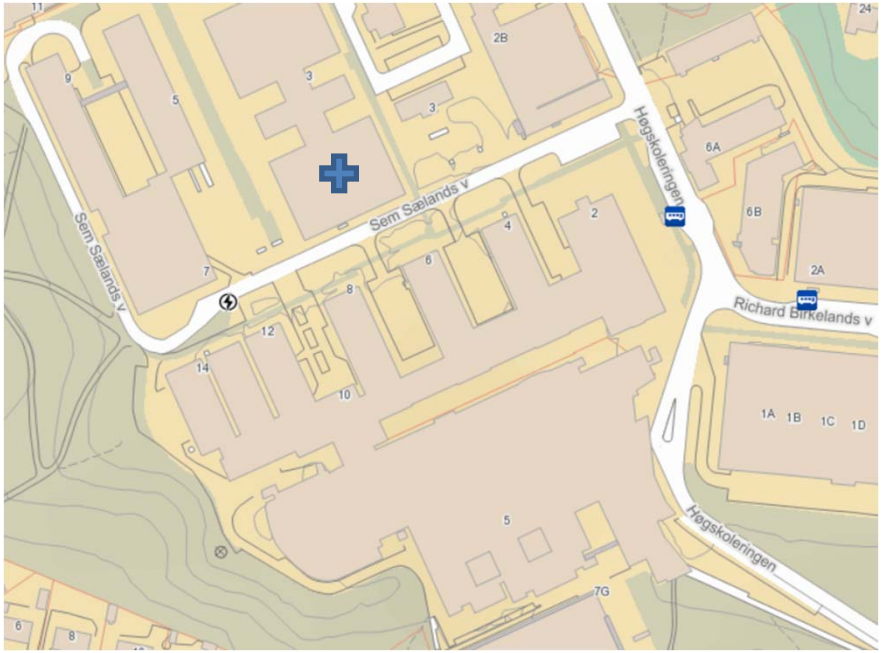
External Funding

- Strong relations to international high-volume industry
- Ambitious strategy for securing external research funding

Thank You!

Lunch 12:00 – 13:00

SIT Kafe Hangaren



Lunch for students sponsored by ARM